Mixed-Signal Radio Receiver

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***Abstract*—A radio frequency receiver front-end for amateur radio operation in the 20-meter (14 to 14.35 MHz) band, was designed and built. An RF filter, low noise amplifier, local oscillator, mixer, ADC, and DSP demodulation blocks were built, implemented, and tested. The RF filter is a broad-band frequency-selective network which attenuates signals outside of the intended frequency range of the radio; a sixth-order Butterworth LC passive lumped-element filter was implemented. To amplify the filtered, received signal, two types of LNAs were built, one using an MMIC and one using a discrete BJT. To create a reference signal for downconversion, a local oscillator was built, using a phase locked loop controlled by a Teensy microcontroller for ease of programming and availability of parts. To downconvert the received radio frequency signal to an intermediate frequency, a passive double-balanced mixer was implemented. To demodulate the downconverted signal, a 1 MHz ADC feeding into an RP2040-based microcontroller (Pi Pico) was used. A circuit board containing the above parts was designed, along with a case and user interface.**

***Index Terms*—Demodulation, Ham radio, Radio receiver**

I. Introduction

A. Background

The field of radio-frequency electronics is a comprehensive application of the vast range of concepts studied as an electrical engineering student: analog electronics, communications theory, signals and systems, and microwave electronics. This project was a study of the application and testing of individual functional blocks, as well as the entire signal-chain of a radio receiver. Not only was it necessary to understand the functionality of a receiver from a signal processing perspective, but it also became critical to study methods of prototyping, testing, and debugging real-world components that are interfaced in a multi-section, cascaded system. The design and testing process was a bridging experience between classroom learning and real-world engineering.

B. Related Work

The ARRL has published multiple books on radio design and construction, usually with a focus on the educational aspect of such work, such as [1], [2], and maintain web resources such as [3]. RF electronics have been extensively documented, in [4], [5], and other texts. The authors' contribution is a single new design, undertaken for educational purposes.

C. Ethical Considerations

While the scope of this project was limited to the receiver of a radio transceiver, general amateur radio practices to transmit and receive signals must follow guidelines set forth by the Federal Communications Commission (FCC). The FCC requires radio amateurs to be licensed and knowledgeable about the rules for legal operation in the United States. Licenses for personal use of amateur stations are granted to individuals of any age upon demonstrating an understanding of relevant FCC regulations and knowledge of radio station operation and safety considerations. Operator licenses are divided into different classes, each corresponding to an increasing degree of knowledge and privileges. These licenses currently remain valid for ten years from the date of issuance or renewal. Details on licenses can be found in [6].

II. RF Front End Design

A. RF Filter

A passive radio frequency (RF) filter was placed in the first stage of the receiver signal chain. This component is required in a heterodyne receiver to prevent undesired signals from being down-converted to the same intermediate frequency (IF) as the desired signal. The desired signal for this project was in the 20-meter band, which spans a frequency range between 14.000 and 14.350 MHz; the pass-band bandwidth of the RF filter was targeted to this same frequency range, necessitating the design of a band-pass filter.

The passive band-pass filter was implemented using a double-tuned filter, shown in figure 1. This structure consisted of two resonators coupled by a capacitor. Each resonator was a parallel inductor (L) and capacitor (C) circuit, in which the capacitor included a trimmer capacitor to adjust the resonant frequency. For each resonator, this frequency was set at the lower and upper pass-band frequencies.

Fig. 1. Circuit diagram of the passive RF band-pass filter.

Because the filter was the first device in the cascaded signal chain, it was critical that it maintained a low noise figure; as shown with Friis's formula, the first device's noise figure determines the best-case noise performance of the overall system [5]. A passive filter's noise figure is equivalent to its

insertion loss. The double-tuned filter was selected not only as it provided greater stop-band attenuation, but also as the tuneable resonant frequencies allowed for a wider pass-band. This result translated to lower losses than a single-tuned circuit over a larger bandwidth, improving noise performance over the entire 20-meter band.

Another consideration as the first functional block in the signal chain was to ensure that the filter's input and output impedances were matched to the antenna and subsequent blocks at 50 Ω. Figure 1 also shows how the input and output impedances were tuned to 14 MHz: The secondary 50 nH inductors were wound on the same toroidal core as the resonant inductor to create matching transformers at the filter ports.

B. Low-Noise Amplifier

The low-noise Amplifier (LNA) serves as a pivotal component in receiver architectures, tasked with amplifying weak incoming signals while minimizing additional noise. Its design significantly influences the receiver's sensitivity, dynamic range, and ability to discern signals amidst noise and interference. Therefore, optimizing the trade-off between gain, noise figure, and linearity is essential for robust receiver performance in challenging communication environments.

1) Design Considerations: The noise figure (NF) of the LNA, quantifying the degradation in signal-to-noise ratio (SNR), is crucial for discerning weak signals amidst noise. Cascaded LNAs in receiver architectures necessitate careful consideration of the total noise figure, calculated using Friis's formula [5], emphasizing the importance of minimizing the noise figure of the initial LNA stage.

LNA gain plays a critical role in determining receiver noise figure, as higher gain minimizes subsequent stages' noise contribution. However, this gain-noise trade-off must be carefully balanced to mitigate non-linear effects and ensure optimal receiver performance.

The 1 dB compression point and gain characteristics of the LNA are vital for shaping receiver linearity and dynamic range. The 1 dB compression point marks the onset of gain saturation and non-linear behavior, impacting the amplifier's linear operating range and signal fidelity. Meanwhile, the gain determines the LNA's ability to amplify weak signals while minimizing noise contribution. Achieving an optimal balance between gain and linearity is essential for maximizing receiver performance [7].

In summary, meticulous design and characterization of the LNA are imperative to ensure optimal sensitivity, dynamic range, and linearity, thereby enabling effective signal detection and processing in modern communication systems.

2) Design Methodology and Results: Two implementation methods were employed for the LNA design: utilizing discrete transistors and utilizing an integrated circuit (IC). Both approaches were explored to evaluate their performance and suitability for the project.

a) Method 1: Designing Using Discrete Transistors: The LNA was designed using the 2N222 NPN bipolar junction transistor (BJT) and the 2N2907 PNP bipolar junction transistor to provide insight into the fundamental design principles and to be able to tailor the amplifier characteristics. Figure 2 depicts the circuit diagram of the LNA.

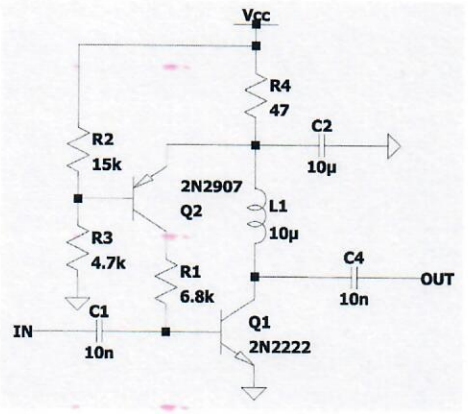

Fig. 2. Circuit diagram of the LNA designed using discrete transistors.

A common-emitter amplifier topology was selected to attain high gain for the LNA. Proper biasing of bipolar transistors is essential to ensure correct operation and to maximize the common-emitter current gain, denoted by β, in the forward-active mode. In this design, the collector-emitter current is approximately proportional to the base current, albeit significantly amplified, for small variations in the base current. To stabilize the operating point against fluctuations in β and V_{cc}, a collector feedback bias scheme is employed, leveraging negative feedback.

Traditionally, resistors are utilized to establish an adequate voltage drop between the base and collector terminals of the transistors. However, resistors introduce substantial thermal noise, thereby impacting the NF of the LNA. To mitigate this, the conventional resistor biasing approach is substituted with a 2N2907 PNP BJT configured as a current source, providing the necessary base current for the 2N222 transistor.

The gain of the common-emitter amplifier is closely linked to its output resistance. In this context, an inductor is employed at the collector of the 2N222 transistor for two primary reasons. Firstly, resistors inherently produce more noise, thereby compromising the NF of the amplifier. Secondly, inductors exhibit high impedance at higher frequencies, contributing to improved amplifier performance in the 20-meter band.

AC simulations were conducted to analyze the performance of the designed LNA, as illustrated in Figure 3.

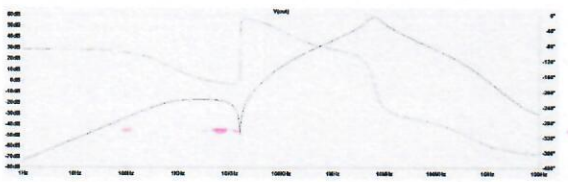

Fig. 3. AC simulation results of the LNA designed using discrete transistors.

b) Method 2: Utilizing BGA616 Chip: The BGA616 integrated circuit presents an alternative to discrete transistor designs, offering advantages in broadband matching and compactness. This chip, designed as a broadband-matched general-purpose monolithic microwave integrated circuit (MMIC) amplifier in a Darlington configuration, exhibits the following key characteristics [8]:

- Broadband operation with a 3 dB bandwidth from DC to 2.7 GHz.
- Typical power gain of 20.0 dB at 100 MHz.
- Typical noise figure of 2.2 dB at 100 MHz.
- Output power at 1 dB gain compression of 18 dBm.

Employing the BGA616 chip provides an efficient solution for achieving the desired LNA performance, ensuring consistency and reliability inherent to integrated circuits. However, challenges arise in adjusting the LNA characteristics when faced with unexpected results.

Amplifiers, particularly those utilizing feedback, may experience instability under varying source and load impedances. In our implementation, connecting the BGA616 after the RF filter on a breadboard led to instability, manifesting as an oscillation at the output. This instability occurs when the gain of the BGA616 exceeds 0 dB and the phase of the output aligns with the input, indicating the presence of unexpected positive feedback within the circuit.

C. Mixer

As a heterodyne receiver, the device must first down-convert the RF signal into an intermediate frequency. While it is possible to directly down-convert the RF signal into base-band audio frequencies, direct conversion poses the challenges of creating sharp filters to prevent image frequencies from being mixed as well. As the 20-meter band spans a larger bandwidth than the signal bandwidth, this design would necessitate another image-rejection filter at the RF stage. Conversely, a relaxed intermediate-frequency allows an analog filter with reasonable sharpness in frequency response to filter any image signals before being mixed.

This mixer was used to multiply the RF signal with a tuneable local oscillator to produce a constant IF signal at 455kHz, which was selected as a standard IF for early analog radios [9]. Though an active mixer (implemented using transistors) is able to provide conversion gain and relax the power requirements for the subsequent IF amplifier, a passive mixer was selected for its simplicity and improved RF and LO port feed-through leakage.

The ADE-1+ is a passive double-balanced mixer with a diode ring structure, shown in figure 4. It was chosen for its improved conversion loss than typical passive mixers and ability operate at frequencies appropriate for the 20-meter band. It comprises of two baluns, or transformers that convert balanced to unbalanced signals. (A signal is *balanced* if it is transmitted along two lines with voltage inversion, created by the center-tapped node in each transformer). In between these two baluns is a diode ring with two paths, each of which is switched on or off according to the driving LO voltage.

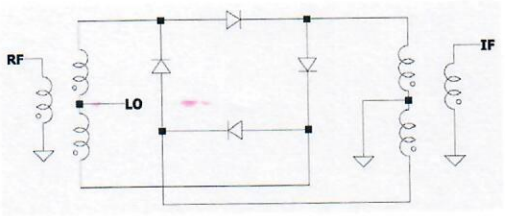

Fig. 4. The passive diode-ring mixer [10].

As recommended by the manufacturer [11], the power of the local oscillator was required to be 10dB larger than the received RF power; a larger LO drive voltage would allow the diode-based switching mechanism to behave more like an ideal square wave.

D. Local Oscillator and Phase-locked Loop

The local oscillator is how a heterodyne receiver tunes to a particular frequency. If an incoming radio signal at frequency ω and a local oscillator signal at frequency ω_l are mixed, this results in output frequencies at $\omega \pm \omega_l$; by low-pass filtering the output, only the frequency at $\omega - \omega_l$, the intermediate frequency, is passed through. If the local oscillator is tuneable, this allows the IF stage to operate at a fixed frequency, improving IF filter selectivity and thus channel selectivity (and simplifying design).

A tuneable local oscillator was designed to drive the mixer according to the designs in [5]. The oscillator consists of a phase-locked-loop (PLL) and a frequency reference. The loop consists of a CD74HC4046BE phase-locked-loop chip and a SN74LS163 binary counter for 16x frequency multiplication. This multiplies the frequency reference, an 875 kHz tuneable pulse-width-modulated (PWM) signal generated by the Pico, into a 14 MHz signal suitable for converting RF into IF. The original version of the PLL had 32x multiplication, but this was found to produce unacceptably high phase noise. Further work would include stabilizing the output frequency of the PLL through use of a more stable voltage-controlled oscillator (VCO).

III. IF Stage Design

After the RF Front-end down-converted the RF signal into an intermediate frequency, the IF stage focused on providing appropriate signal levels to be interfaced with the digital micro-controller. The appropriate signal level necessitate the following general considerations:

- A clean signal with no spurious products from the mixer.
- Enough voltage amplification from the RF signal to utilize full bit depth of the analog-to-digital converter.
- Proper sampling of analog signal to interface with the micro-controller.

A. IF Filter

The aforementioned mixer was driven by a square-wave oscillator at 1.4Vpp amplitude, which is much larger than general RF signal levels. Not only would the mixer output

higher-order spurious multiplication products, but also the higher-order harmonics of the LO would be present at the IF output as well. The first task following the RF mixer was to filter out these spurious components using an IF filter.

The IF filter was selected for pass-band around $f_c = 455$ kHz. As SSB demodulation for audio reception require at least 3 kHz signal bandwidth, this filter necessitated a high Q-factor, or sharpness, in response. To implement this filter, two possible approaches included:

- Method 1: Using a discrete band-pass filter at 455 kHz with the narrowest bandwidth available in production.
- Method 2: Using a discrete 455 kHz crystal resonator, with an ideal narrow-band resonant frequency.

As shown above, the primary consideration when selecting the IF filter was the pass-band bandwidth. From the available components in the market, the best discrete filter had a 6 dB-passband bandwidth of $f_c \pm 6kHz$. Meanwhile, the resonator selected had a frequency tolerance of $f_c \pm 2kHz$.

After lab measurements, the LTC455FU crystal filter was selected over the ZTB455E crystal resonator. While the filter had a larger 3 dB bandwidth at 8.1kHz over the 5.1kHz bandwidth of the resonator, the filter offered improved stop-band attenuation at 26 dB over the resonator's 23 dB.

However, this filter was manufactured at input and output impedances of 1.5 kΩ, substantially larger than the mixer's 50 Ω output. The filter must ideally convey all the input power into its output, as it is placed before voltage gain by the subsequent IF amplifier. For maximum power transfer, this filter necessitated a matching network to transform its high input impedance to the 50 Ω source impedance.

The design of this matching network was facilitated by the relatively low operation frequency of 455 kHz, which allowed lumped-element networks to provide reasonable performance over the narrow 3 kHz bandwidth. There were two options for lumped-element matching networks:

- Method 1: L-section, using a single-section series and parallel inductor and capacitor configuration.
- Method 2: Transformers, using the turns ratio to adjust the impedance - and hence, the voltage - at the primary and secondary coils. Matching transformers were used in the input and output of the Rf filter as well.

For ease of testing, the L-section matching network was built at the input and output of the IF filter. This matching network is displayed in figure 5.

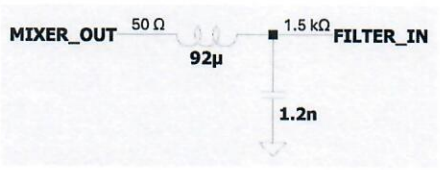

Fig. 5. Lumped L-section matching network for the IF filter.

Upon tests with the spectrum analyzer, there was significant improvement in insertion loss, which is displayed in the following measurement results.

B. IF Amplifier

The intermediate frequency (IF) amplifier is a crucial component in the receiver architecture, responsible for amplifying the signal at the intermediate frequency stage before further processing. Its primary objective is to provide sufficient gain to ensure accurate sampling by the analog-to-digital Converter (ADC), facilitating precise signal demodulation and decoding.

1) Design Considerations: The design of the IF amplifier necessitates careful consideration of several factors to meet the system's performance requirements. One crucial consideration is the need for sufficient gain to ensure the IF signal is adequately amplified for precise sampling by the ADC. Additionally, the amplifier's bandwidth and linearity are essential to preserve signal integrity and minimize distortion.

2) Design Methodology and Results: Two implementation methods were explored for the IF amplifier: utilizing the MC1350 IC and cascading 2N222 transistors to form a custom amplifier.

a) Method 1: Utilizing MC1350 Chip: The MC1350 integrated circuit is a versatile component widely used in radio frequency (RF) and intermediate frequency (IF) amplifier applications. Its internal architecture comprises multiple transistor stages arranged in a cascode configuration, facilitating high-gain amplification and it exhibits the following characteristics [12]:

- 3 dB bandwidth of 20 kHz.
- Typical power gain of 62 dB at 455 kHz.

The MC1350 IF amplifier employs a differential cascade amplifier configuration, as depicted in Figure 6. Q1, Q2, Q3, and Q6 form the differential cascode amplifier. With a positive AGC bias voltage applied to the bases of Q4 and Q5, they conduct and shunt away the signal current of Q3 and Q6, attenuating the gain of the amplifier. The differential output is taken from the collectors of Q8 and Q9 [13].

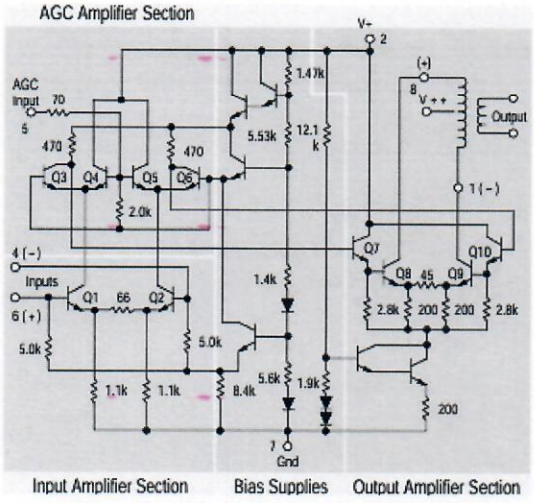

Fig. 6. Circuit schematic of MC1350.

To measure the power gain at 455 kHz, the circuit configuration shown in Figure 7 is utilized. Single-ended output is taken

from the collector of Q8 while the unused collector of Q9 is connected to the positive supply V^+. Operation in this mode reduces the circuit gain [13]. Also, the single-ended input is applied to Q1 while the base of Q2 is grounded through a capacitor.

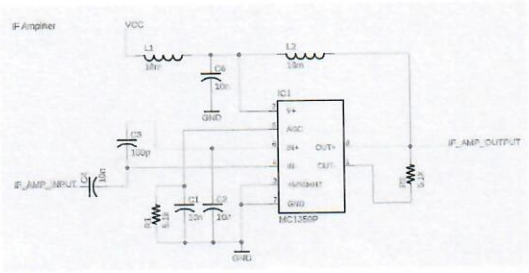

Fig. 7. Power gain test circuit of MC1350.

The MC1350 integrated circuit offers a convenient and efficient solution for IF amplification in RF systems. Its wide range of automatic generation control (AGC) and high gain characteristics make it suitable for various applications requiring IF amplification.

b) Method 2: Designing Using Discrete Transistors: In addition to the IC approach, a custom amplifier was constructed using cascaded 2N222 transistors. This approach provided flexibility in designing the amplifier characteristics to meet specific project requirements. By carefully selecting component values and configuring the transistor stages, we were able to achieve the desired gain and performance parameters for the IF amplifier.

C. Analog-to-Digital Converter

An analog-to-digital converter (ADC) operating at 1 Msps was employed to digitize the amplified 455 kHz IF signal in preparation for demodulation. We used an AD7478, an 8-bit resolution successive approximation ADC from Analog Devices [14], as it has sufficient bit depth to digitize our signal. Our sampling rate was chosen to place the Nyquist frequency significantly higher than 455 kHz to ensure exact capturing of the IF signal. ADC data is read onto the Pico over SPI via a direct memory access (DMA) bus to save processor cycles; DMA was a driving force behind using an RP2040-based microcontroller for this radio.

IV. Digital Signal Processing

ADC data is read through SPI DMA and processed on the Pico. The incoming data is digitally rectified to perform double-sideband (DSB) demodulation and optionally passed through an elliptic filter to remove unwanted mixing products. Our chosen IF and Nyquist frequency (455 kHz and 500 kHz, respectively) cause products to appear at ± 90 kHz when mixing digitally, which is out of range for human hearing but may pose issues with future DSP work. The demodulated signal is downsampled by a factor of 4 and played over PWM. DMA is also used for audio playback. Digital single-sideband modulated (SSB) signal demodulation, as described in [15] and [16], is possible using a similar architecture.

One practical issue with audio demodulation was that the SPI DMA reads and PWM DMA audio playback writes would not finish at the same time, due to the limited frequency resolution of the Pico's internal frequency synthesizer. This caused "clicks" in the audio playback after each buffer of data due to the audio output dropping to zero at the end of its buffer. This was solved by inserting enough duplicate samples throughout the playback to cause the buffers to finish at the same time.

V. Printed Circuit Board Design

Prototype assembly was conducted on a mixture of breadboards and perforated circuit boards. Once each device's functionality was tested both individually and as a whole, a Printed Circuit Board (PCB) was designed to provide various improvements to the physical construction of the electronic system. While breadboards are a useful prototyping tool because of the speed at which connections can be made, they suffer from significant parasitic capacitance between adjacent rows. Perforated boards do not suffer from the same parasitic capacitance and are also modular, but do not support the footprints of the surface-mount devices we selected for our design. Besides less significant parasitic effects and surface-mount footprint support, the custom PCB offers other benefits such as mechanical mounting and high component density. Our PCB is a two-layer design which will be fabricated on 1.6mm thick FR-4 material, a glass-fiber laminate commonly used in circuit board assemblies. While the operating frequencies present in our system are not high enough to warrant a distributed-element approach to board layout, care was taken to prioritize short trace lengths, especially in the RF portion of the circuit. The design also features single-layer signal routing and a ground plane throughout, which should aid in mitigating both capacitive and inductive coupling between traces, and provide a nearly best-case path for return current. At the time of writing, the board has been designed but has not yet been received, so tests have not been performed. After receiving and assembling of the PCB, the signal chain will be tested block by block, just as it had been in the prototype assembly.

VI. Measurements

A. RF Front End

B. IF Stage

C. DSP Stage

Ideal audio fidelity was tested informally by playing back a synthesized 110 Hz and 165 Hz signal simultaneously. Actual fidelity of the digital demodulation stage was tested by feeding a DSB modulated 455 kHz signal, synthesized by a function generator, directly into the ADC and examining the noise and spurious frequencies in the audio output. This method was limited by unusual frequency components in the function generator's own output, causing unexpected tones to appear in the audio playback in addition to the main (modulating) tone.

VII. Conclusion

A. Future Work

Analog SSB demodulation would be an excellent extension to this project. It would require a more stable local oscillator, likely employing a discrete crystal reference and frequency synthesizer.

Acknowledgment

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